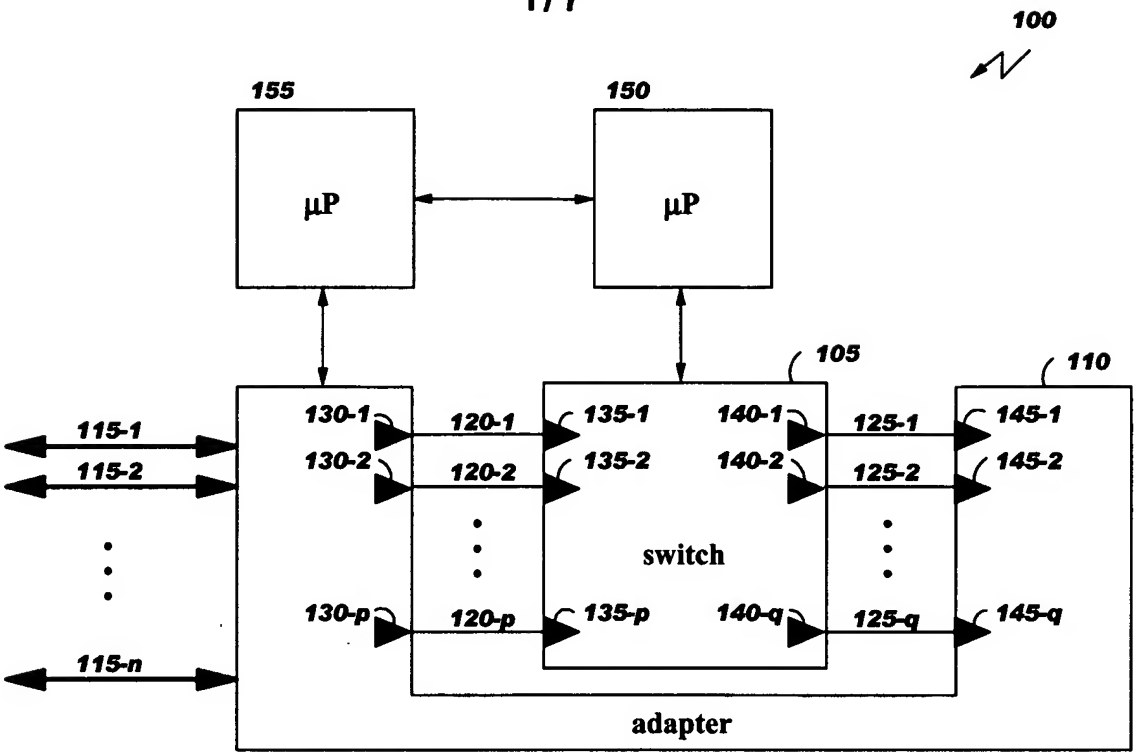


Figure 1

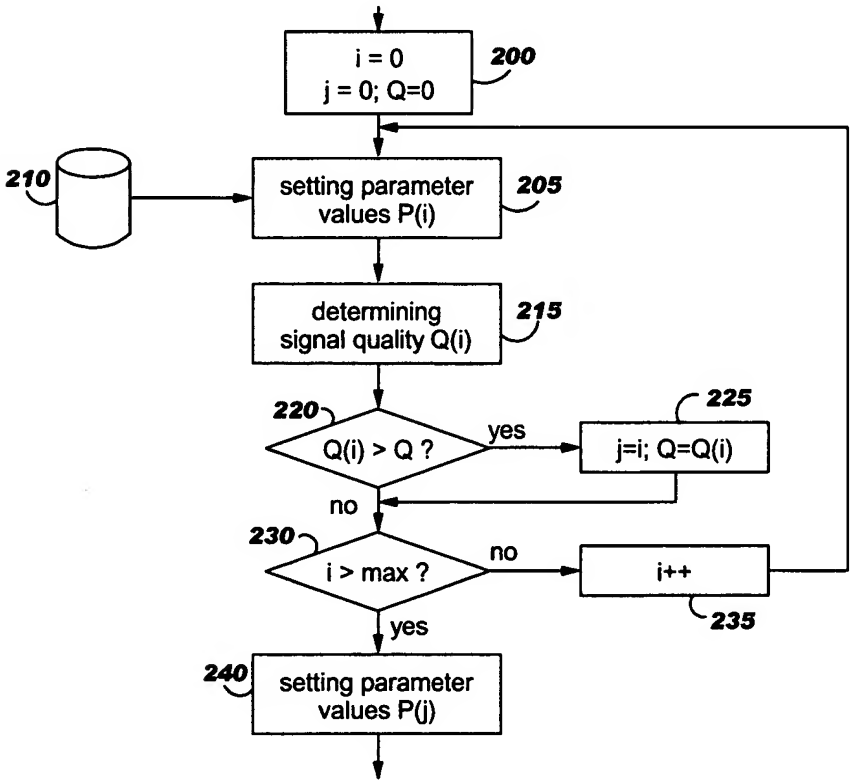


Figure 2

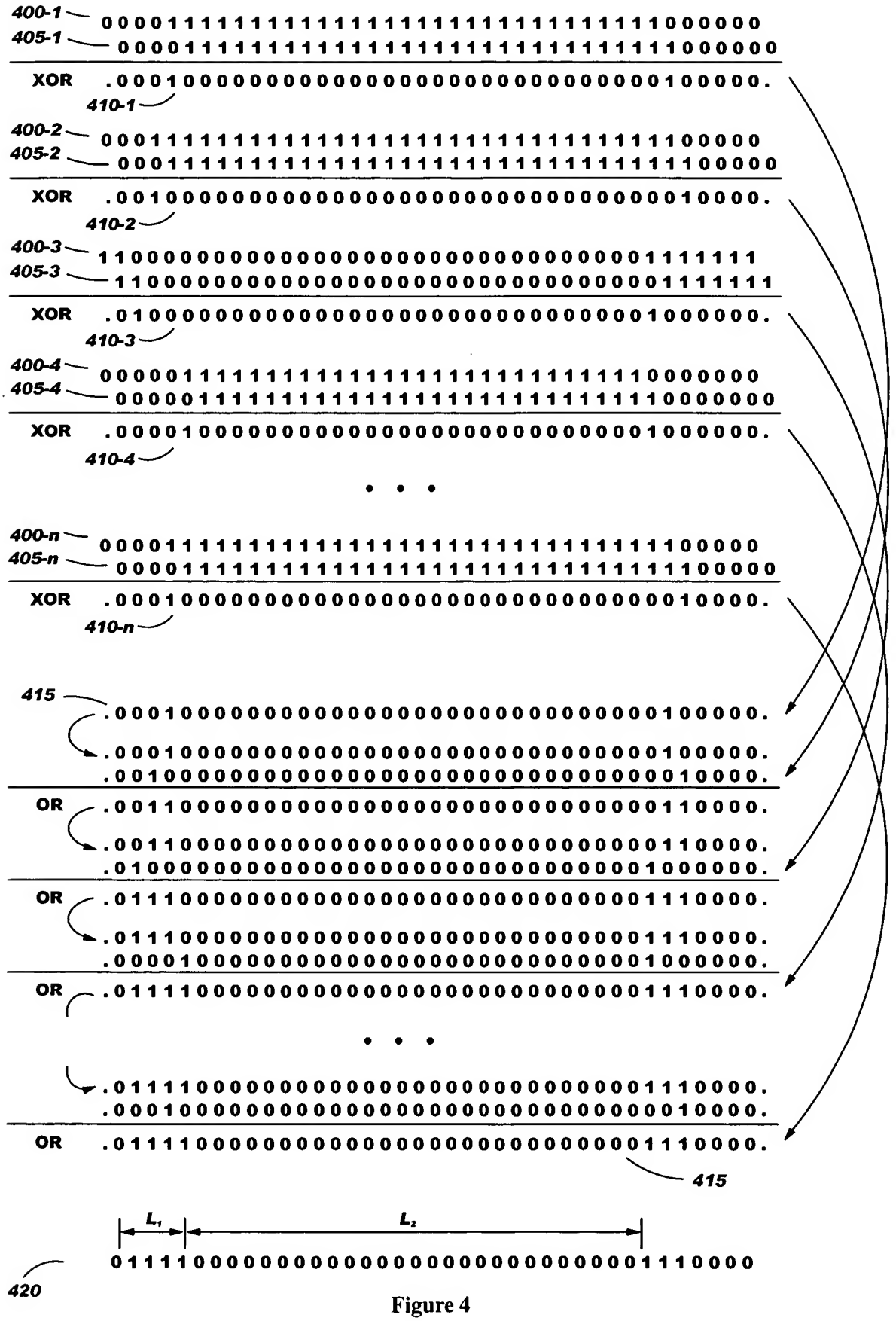

400-1
405-1
XOR
410-1
400-2
405-2
XOR
410-2
400-3
405-3
XOR
410-3
400-4
405-4
XOR
410-4
400-n
405-n
XOR
410-n
415
OR
OR
OR
415
L1
L2
420

Figure 4

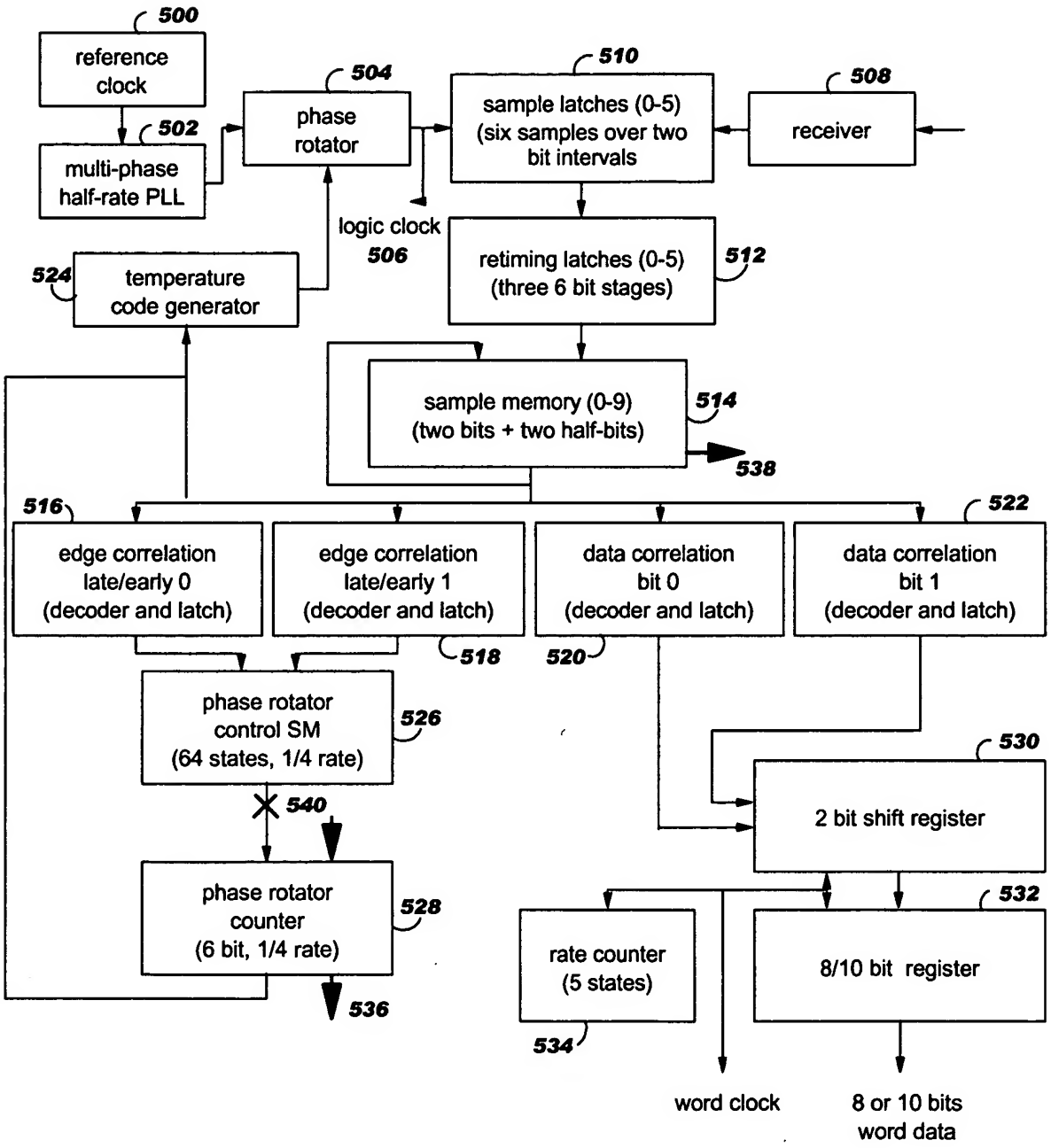

500
reference clock
502
multi-phase half-rate PLL
504
phase rotator
logic clock
506
510
sample latches (0-5) (six samples over two bit intervals
508
receiver
512
retiming latches (0-5) (three 6 bit stages)
524
temperature code generator
514
sample memory (0-9) (two bits + two half-bits)
538
516
522
edge correlation late/early 0 (decoder and latch)
edge correlation late/early 1 (decoder and latch)
518
data correlation bit 0 (decoder and latch)
520
data correlation bit 1 (decoder and latch)
526
phase rotator control SM (64 states, 1/4 rate)
530
2 bit shift register
540
528
phase rotator counter (6 bit, 1/4 rate)
532
rate counter (5 states)
8/10 bit register
536
534
word clock
8 or 10 bits word data

Figure 5

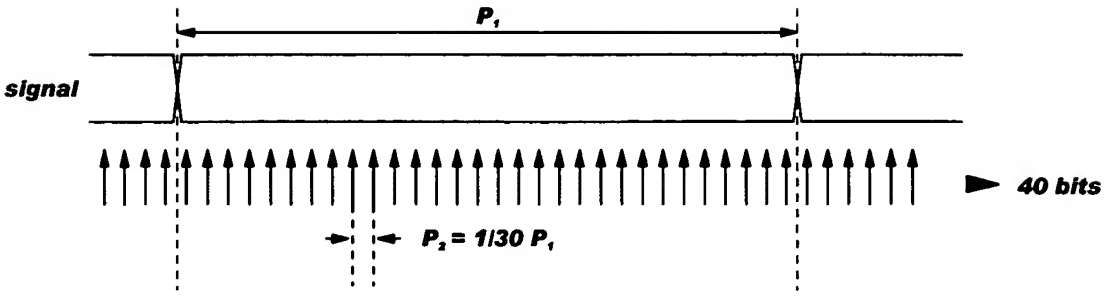


Figure 3

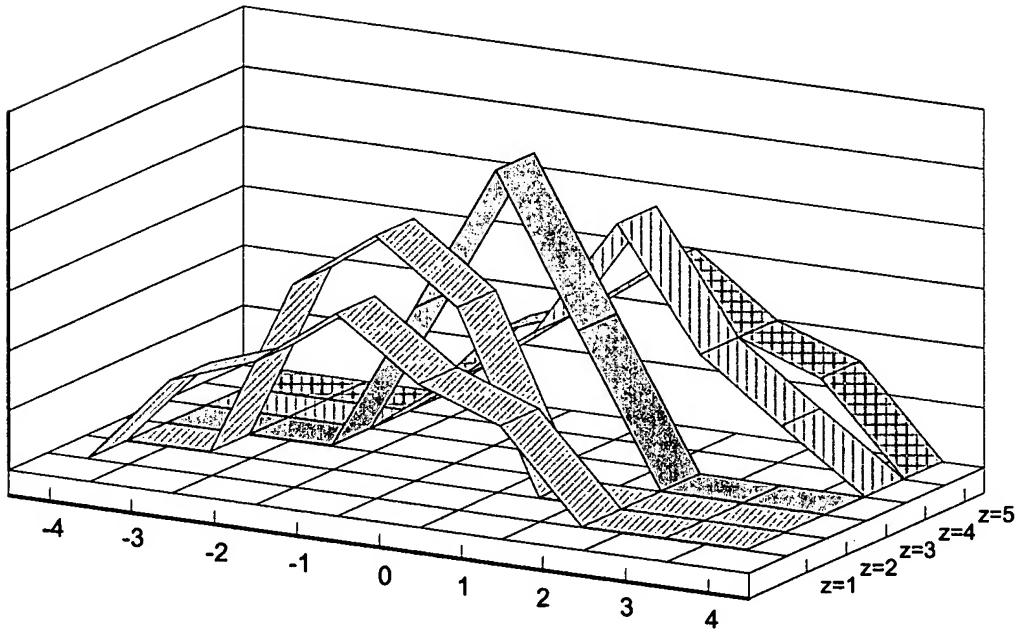


Figure 6

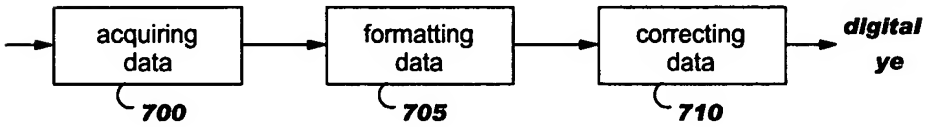


Figure 7

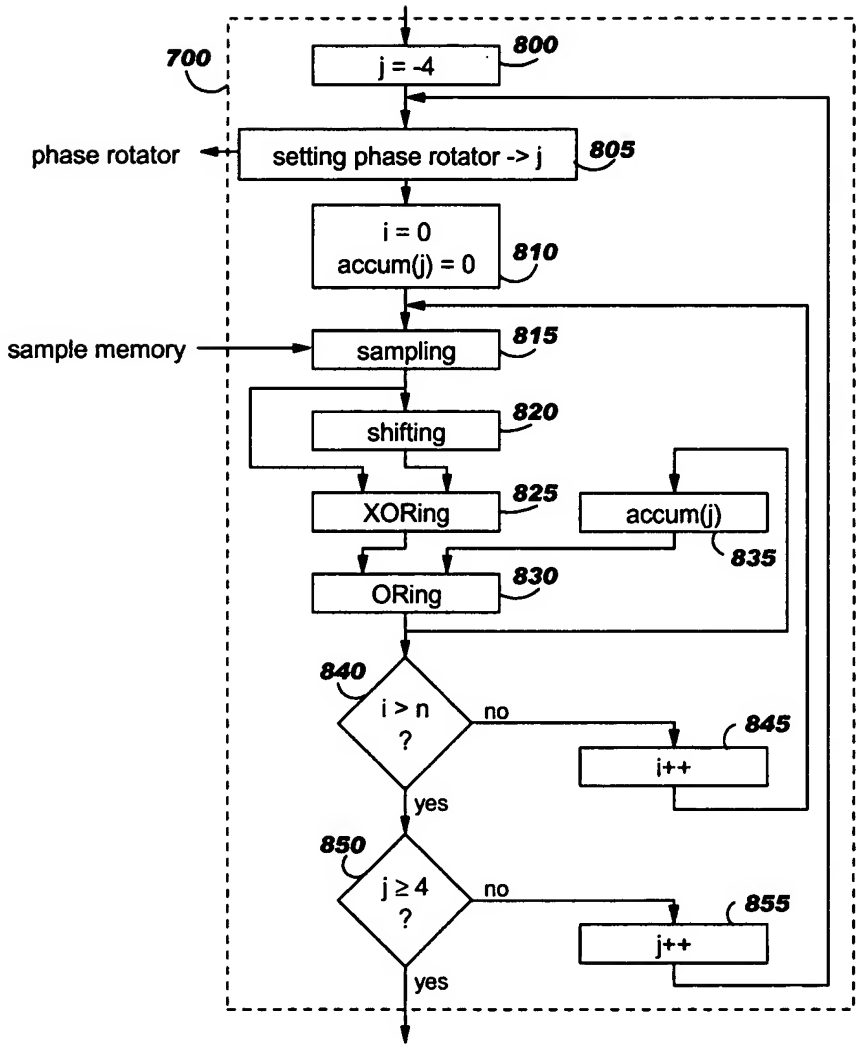

700
j = -4
800
phase rotator
setting phase rotator -> j
805
i = 0
accum(j) = 0
810
sample memory
sampling
815
shifting
820
XORing
825
accum(j)
835
ORing
830
840
i > n
?
no
845
i++
yes
850
j ≥ 4
?
no
855
j++
yes

Figure 8

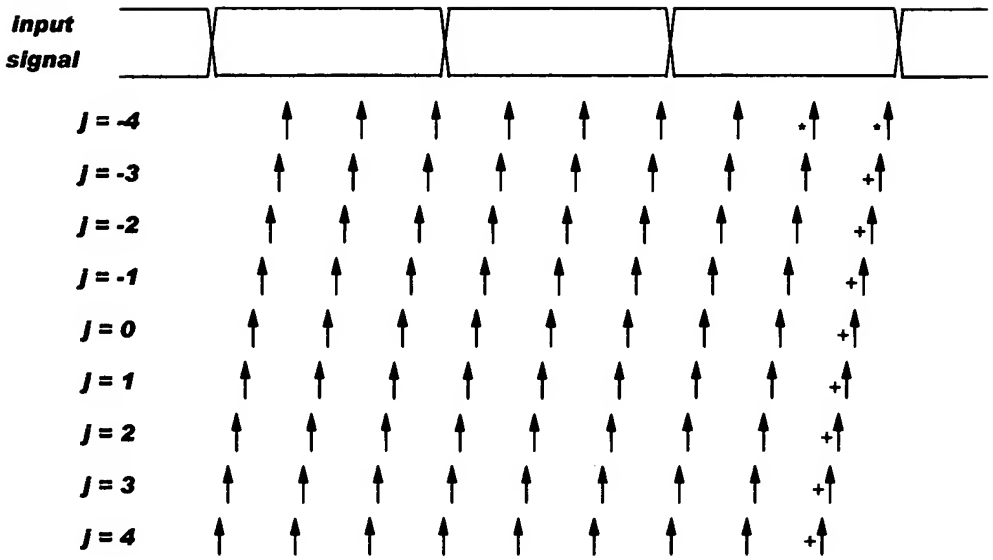
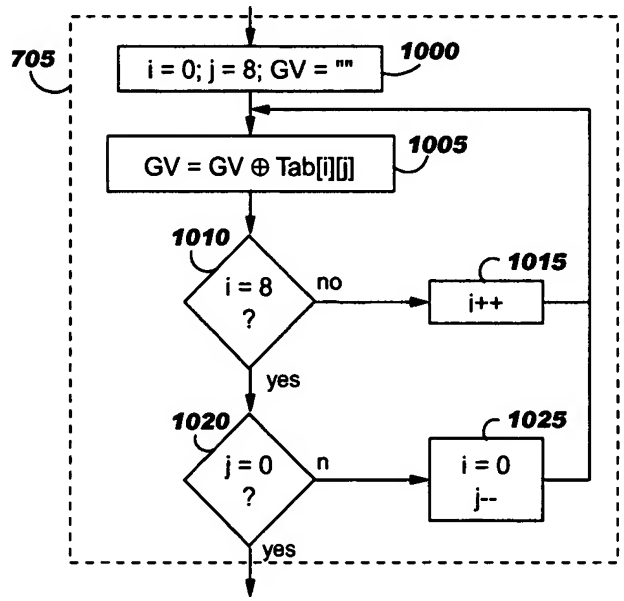


Figure 9a

Pos./Bit	0	1	2	3	4	5	6	7	8
j = -4	1	1	0	0	1	0	1	1	0
j = -3	1	1	0	0	1	0	1	1	0
j = -2	1	1	0	0	1	0	1	1	0
j = -1	1	1	0	0	1	0	1	1	0
j = 0	1	1	0	0	1	0	1	1	0
j = 1	0	1	1	0	1	0	0	1	1
j = 2	0	1	1	0	1	1	0	1	1
j = 3	0	1	1	0	1	1	0	1	1
j = 4	0	1	1	0	1	1	0	1	1

Figure 9b

Figure 10



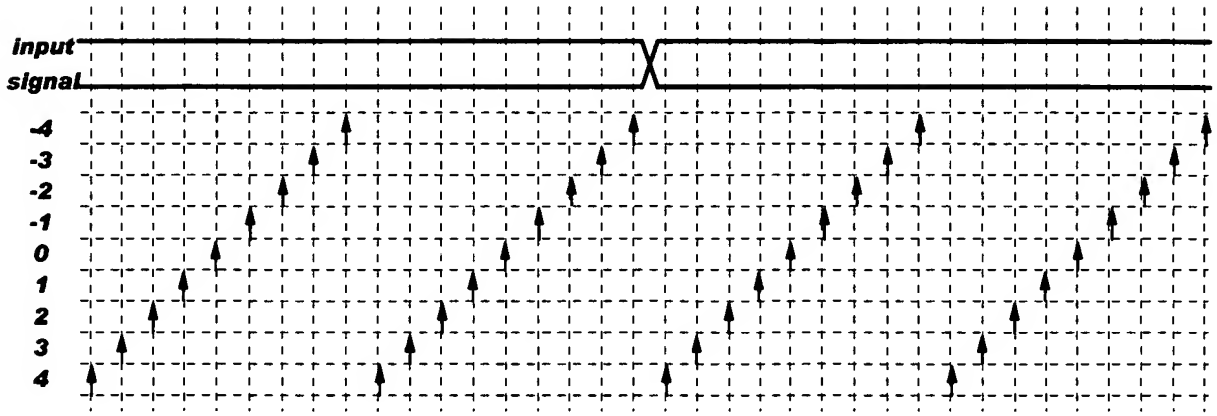


Figure 11

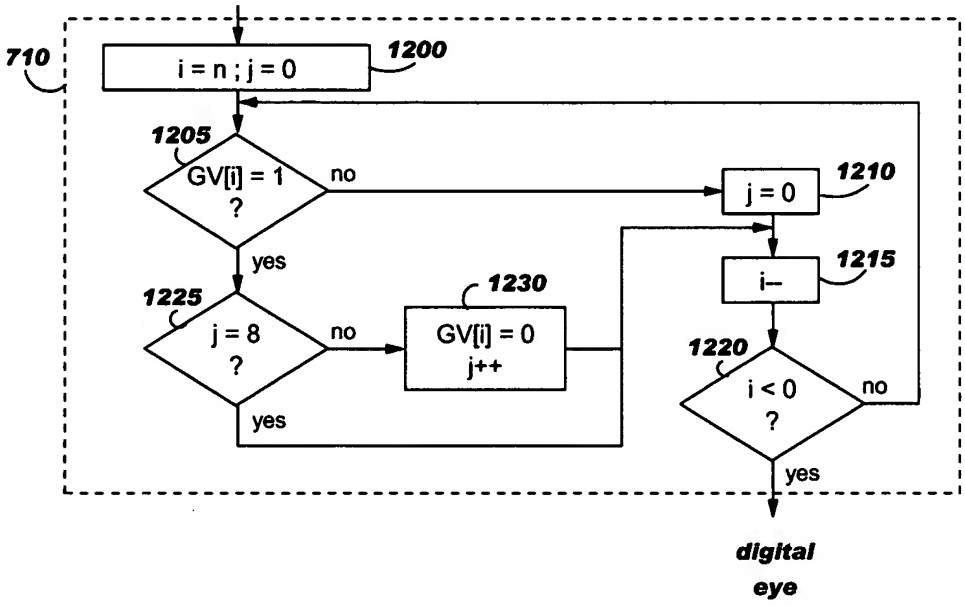


Figure 12

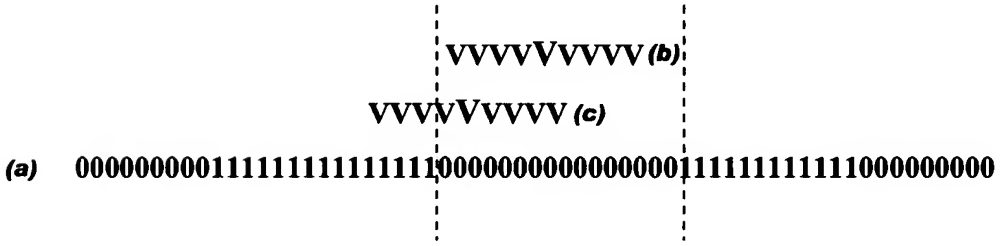


Figure 13